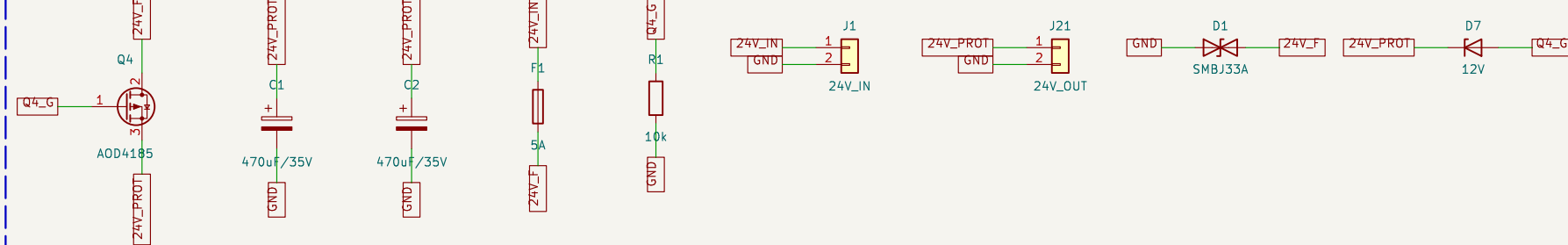
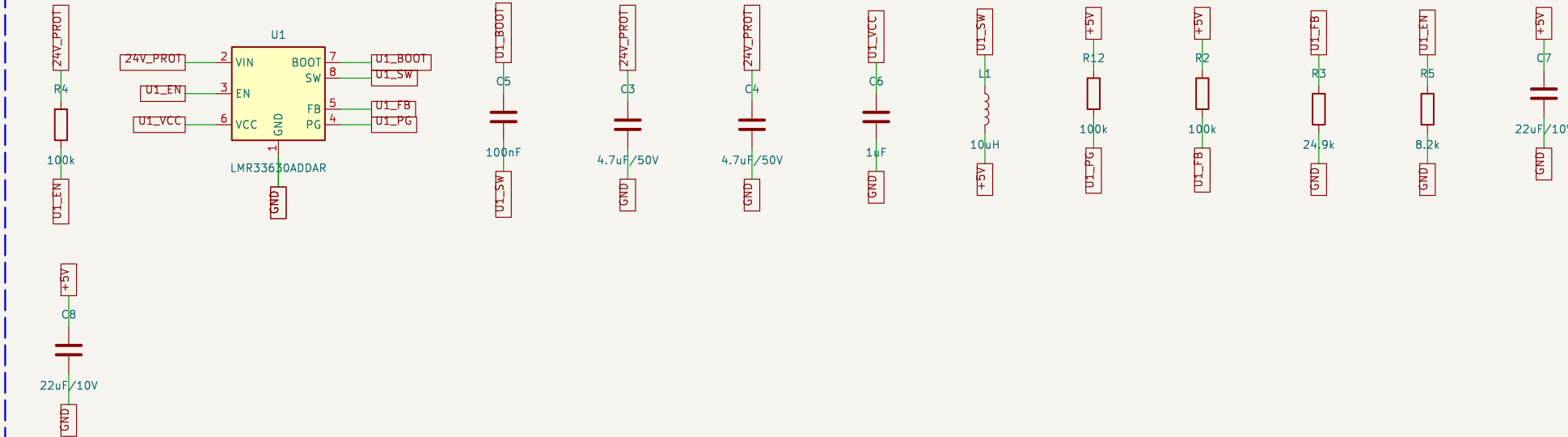


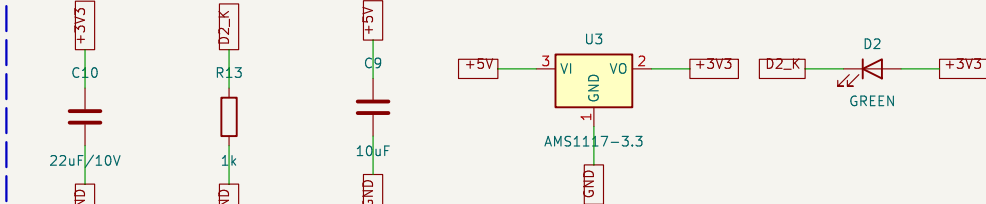
1 24 V input, fuse, TVS, reverse-polarity ideal diode



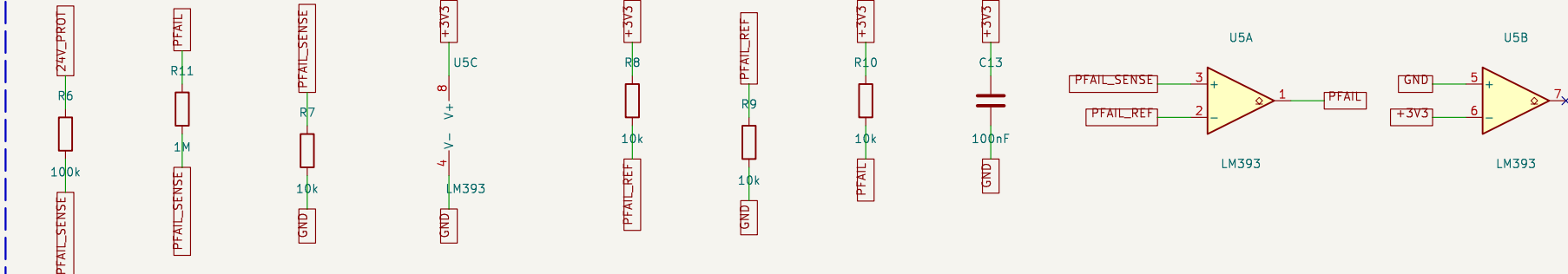
2 24 V -> 5 V synchronous buck (LMR33630, 3 A)



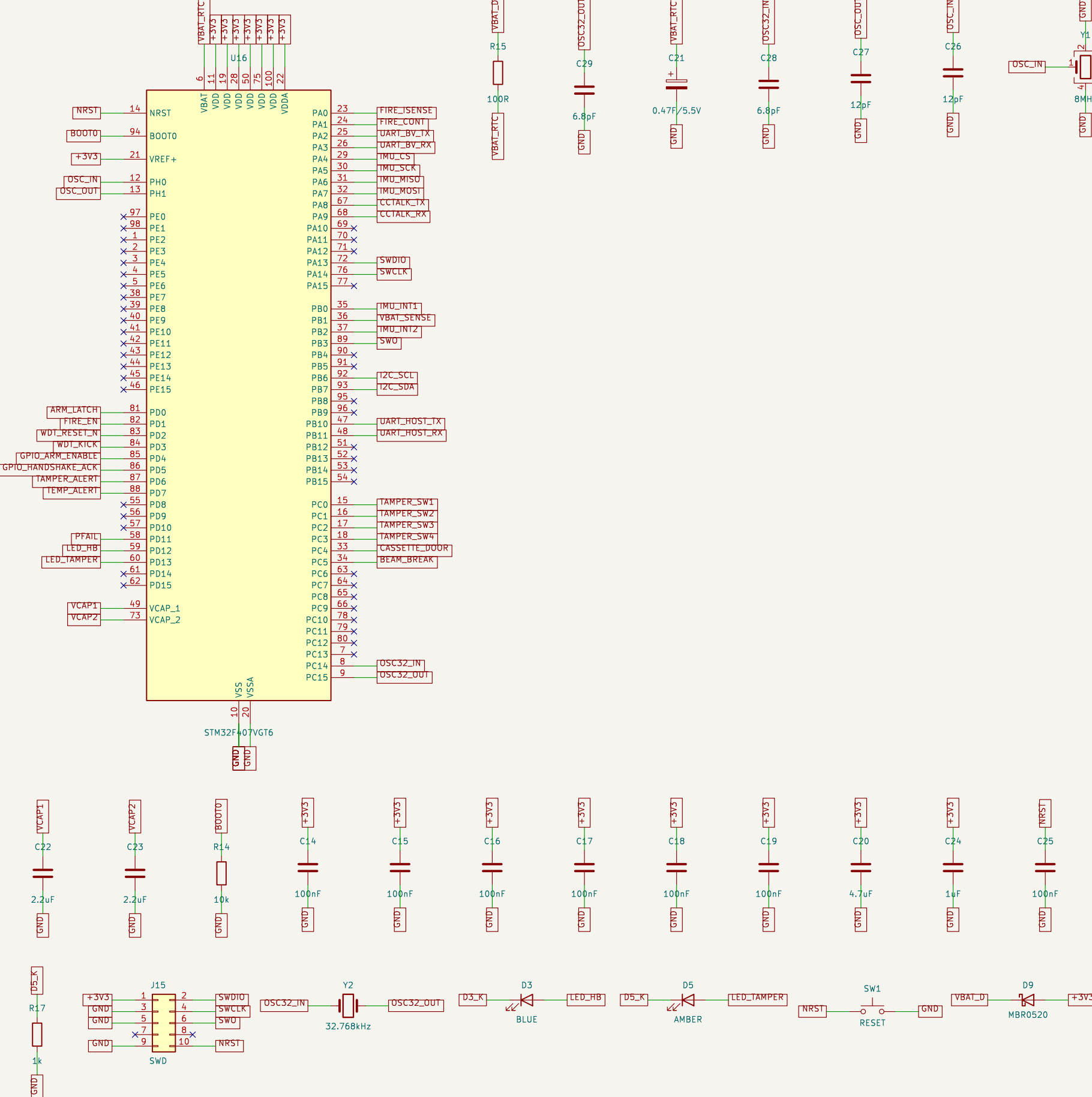
3 5 V -> 3.3 V LDO



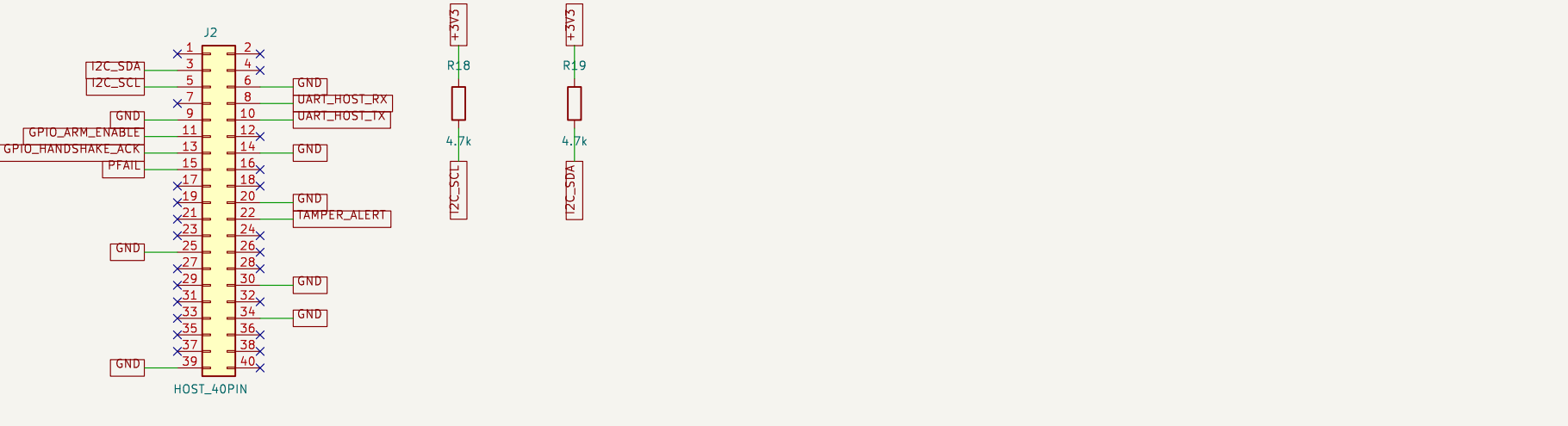
4 Power-fail comparator (trip 18 V, PFAIL active-low)



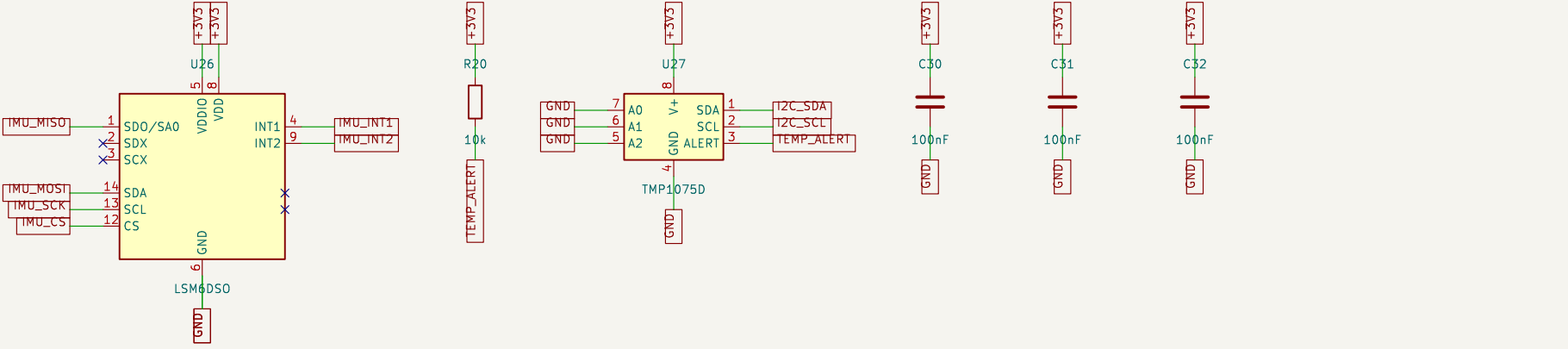
5 STM32F407VGT6 real-time controller, clocks, SWD, RTC supercap



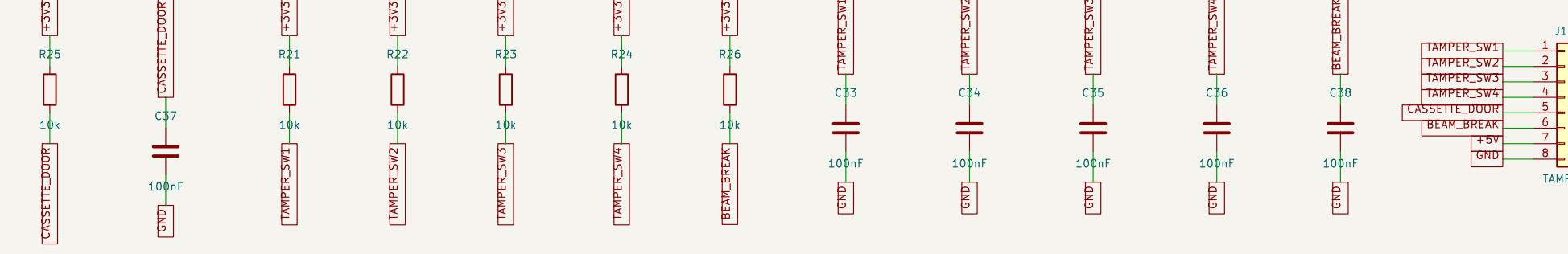
6 Host link to CM4 IO board 40-pin header (3V3 UART/I2C/GPIO)



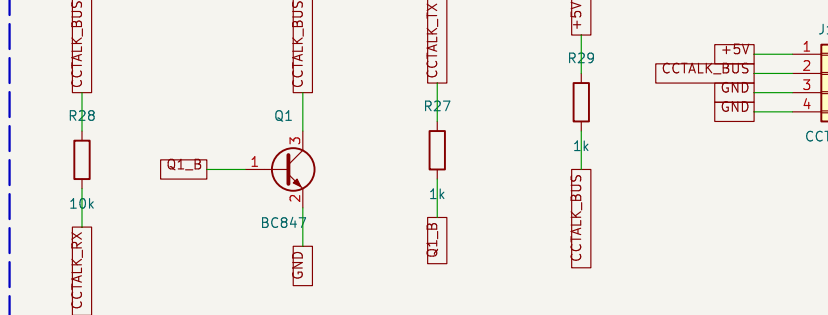
7 IMU (LSM6DSO, SPI1) and board temperature (TMP1075, I2C1)



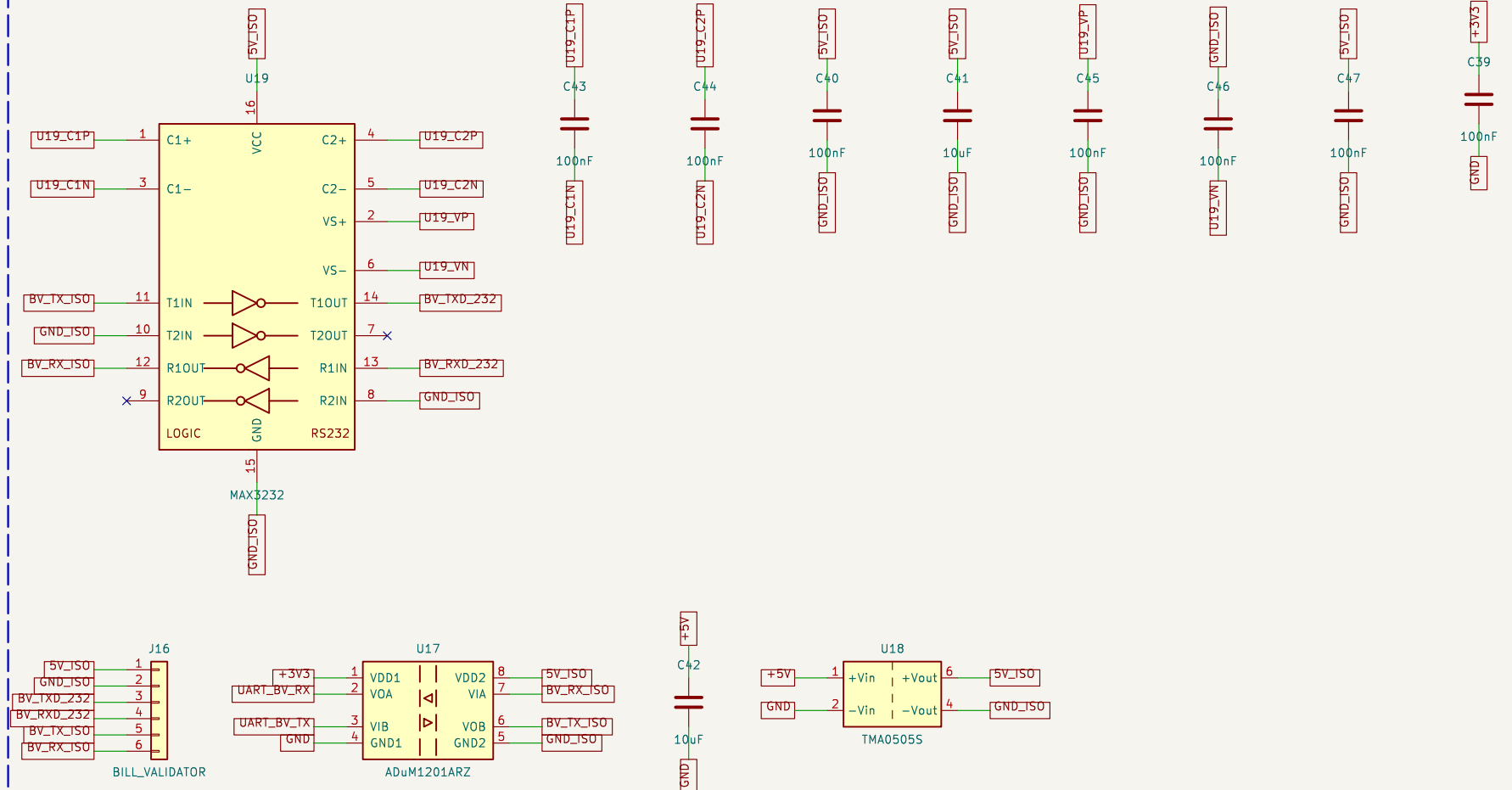
8 Tamper inputs: 4x chassis micro-switch, cassette door, beam-break



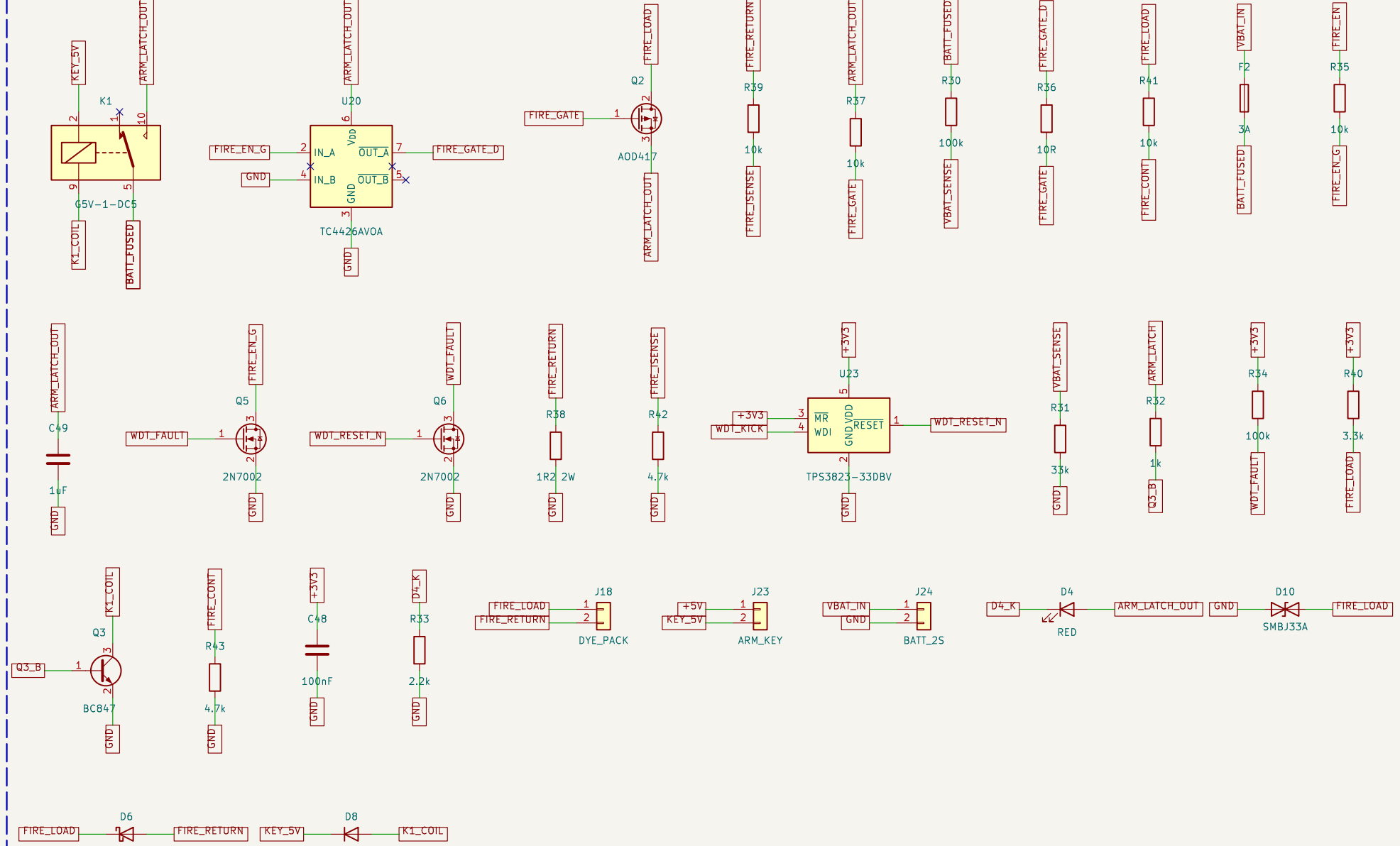
9 ccTalk open-collector bus (USART1)



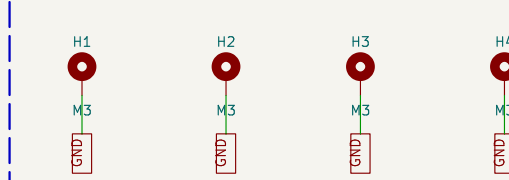
10 Isolated bill-validator UART (ADuM1201 + TMA0505S + MAX3232, ID-003)



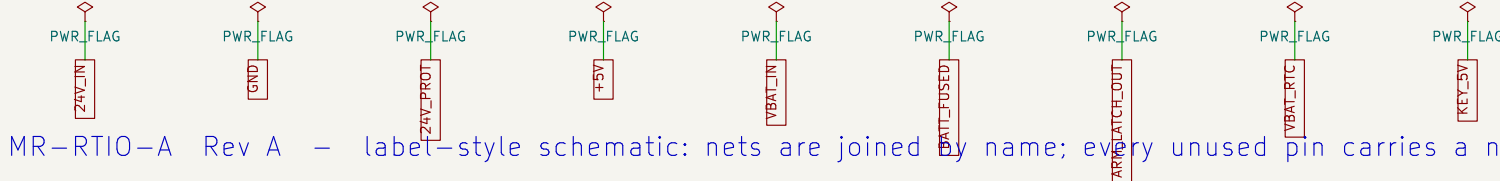
11 Dye-pack ARM / FIRE chain: key relay, watchdog inhibit, P-FET, sense



12 Mounting



Power-flag strip: nets sourced by connectors / passives



MR-RTIO-A Rev A - label-style schematic: nets are joined by name; every unused pin carries a no-connect flag; isolated domain (5V_ISO / GND_ISO) is bridged only by U17 (ADuM1201) and U18 (TMA0505S). Fire chain: KEY -> K1 -> ARM_LATCH_OUT -> Q2 gated by U20 <- FIRE_EN & watchdog OK.